Amendments to the Claims:

Please cancel Claims 28 and 34 and amend Claims 1-4, 6, 8, 10-14, 16-20, 22, 24-27, 29-33, 35-38, 40, and 42-45 as follows:

1. (Currently Amended) A method of identifying a plurality of transponders in an interrogation process comprising:

transmitting an interrogation signal to the transponders; ~~and~~

receiving a response signal from each transponder at a time within a respective waiting period the maximum duration of which can be adjusted;~~, characterised by~~

creating a plurality of data line signals together defining a random number;~~,~~

feeding said data line signals to a counter for determining the waiting period;~~,~~ and

providing at least one of the data lines with logic circuitry whereby control of the logic circuitry can block or permit the data line signal to the counter thereby adjusting the total number of data line signals reaching the input of the counter to control the maximum length of the waiting period.

2. (Currently Amended) A method of identifying a plurality of transponders in an interrogation process comprising:

transmitting an interrogation signal to the transponders; ~~and~~

receiving a response signal from each transponder during a respective waiting period the maximum duration of which can be adjusted, the transponder having a random number generator and a counter;~~, characterised by~~

transmitting output signals from the random number generator to respective inputs of the counter for determining the waiting period, at least one of the output signals from the random number generator being fed via logic circuitry to a respective input of the counter; and

controlling the logic circuitry to adjust the maximum length of the waiting period.

3. (Currently Amended) A method as claimed in claim 1 ~~or claim 2~~, wherein the logic circuitry comprises one or more logic gates, the number of logic gates being less than the number of data lines.

4. (Currently Amended) A method as claimed in ~~any one of claims 1 to 3~~claim 1, wherein the waiting period consists of a plurality of smaller time intervals or time slots together defining a Round Size representative of that waiting period.

5. (Original) A method as claimed in claim 4, wherein there is a minimum Round Size and at least one larger Round Size, the or each larger Round Size consisting of a combination of minimum Round Sizes, whereby controlling the logic circuitry determines the number of minimum Round Sizes to be combined to define the desired larger Round Size to be used.

6. (Currently Amended) A method as claimed in claim 1~~any one of claims 1 to 5~~, wherein by controlling the logic circuitry the maximum duration of the waiting period is increased or decreased by multiples of 2 or 0.5 respectively.

7. (Original) A method as claimed in claim 5, wherein by controlling the logic circuitry the desired Round Size is selected by increasing or decreasing the number of minimum Round Sizes to be combined, the different Round Sizes available being related to one another by factors or multiples of 2 or 0.5.

8. (Currently Amended) A method as claimed in claim 2~~, or in any one of claims 3 to 7 when dependent on claim 2~~, including the step of clocking the random number generator and/or clocking the counter by means of a clock oscillator of the transponder.

9. (Original) A method as claimed in claim 8, including causing the transponder to transmit an output signal from its transmitter when the counter has been counted to its terminal count, whereupon the counter loads a fresh or new number from the random number generator for the next count.

10. (Currently Amended) A method as claimed in ~~claim8 or claim 9~~claim 8, comprising determining the maximum possible waiting time or maximum possible number of slots over which to ~~randomise~~ randomize transmissions of the output signal from the transmitter by the

length of the counter, the data lines between the random number generator and the counter being gated in order "fold" the counter such that the effective counter length may be modified in multiples of two.

11. (Currently Amended) A method as claimed in claim 1 ~~or any of claims 3 to 10 when dependent on claim 1~~, including deriving the random number by taking a snapshot of the transponder clock, or by a hash value received from the interrogator in a command.

12. (Currently Amended) A method as claimed in claim 1 ~~any one of claims 1 to 11~~, including using either an up or a down counter whereby the terminal value of the counter is reached with the clocking signal causing the counter to either increment or decrement as required.

13. (Currently Amended) A method as claimed in claim 1 ~~any one of claims 1 to 12~~, wherein the output response signal contains identity or field data of a tag or transponder.

14. (Currently Amended) A method as claimed in any claim 1 ~~any one of claims 1 to 13~~, wherein transponders not already included in an active population under interrogation are arranged to enter said active population, whereupon said transponders entering the active population receive a signal from the interrogator to adjust the maximum length of their waiting period.

15. (Original) A method as claimed in claim 14, wherein the adjusted maximum length of the waiting period of the transponders, after arriving into an already existing active population under interrogation, is chosen to ensure transmissions from said transponders occur at an appropriate stage in the arbitration to facilitate reading of those transponders entering the active population.

16. (Currently Amended) A method as claimed in claim 14 ~~or claim 15~~, wherein the transponders are moving relative to the interrogator.

17. (Currently Amended) A transponder for generating an output signal during a waiting period, comprising: ~~including~~

means for deriving a random number within the transponder; and

means for delivering the random number by way of binary output signals along a plurality of data lines to a counter, ~~characterised in that~~ wherein at least one of the data lines is connected to the counter via logic circuitry, wherein ~~whereby~~ control of the logic circuitry can block or permit the data line signal to the counter thereby adjusting the total number of data line signals reaching the input of the counter to control the maximum length of the waiting period.

18. (Currently Amended) A transponder for generating an output signal during a waiting period, the transponder comprising: ~~including~~ a random number generator the binary output signals from which are fed to the inputs of a counter for determining the waiting period, wherein ~~characterised in that~~ at least one of the output signals from the random number generator is fed via logic circuitry to a respective input of the counter whereby control of the logic circuitry adjusts the maximum length of the waiting period.

19. (Currently Amended) A transponder as claimed in claim 14 ~~or claim 15~~, wherein the logic circuitry comprises one or more logic gates, the number of logic gates being less than the number of data lines for the binary output signals.

20. (Currently Amended) A transponder as claimed in ~~any of claims 14 to 16~~claim 14, wherein the waiting period consists of a plurality of smaller time intervals or time slots together defining a Round Size representative of that waiting period.

21. (Original) A transponder as claimed in claim 17, wherein there is a minimum Round Size and at least one larger Round Size, the or each larger Round Size consisting of a combination of minimum Round Sizes, whereby controlling the logic circuitry determines the number of minimum Round Sizes to be combined to define the desired larger Round Size to be used.

22. (Currently Amended) A transponder as claimed in claim 14~~any one of claims 14 to 18~~, wherein the logic circuitry is arranged to enable the maximum duration of the waiting period to be increased or decreased by multiples of 2 or 0.5 respectively.

23. (Original) A transponder as claimed in claim 18, wherein the logic circuitry is arranged to enable the desired Round Size to be selected by increasing or decreasing the number of minimum Round Sizes to be combined, the different Round Sizes available being related to one another by factors or multiples of 2 or 0.5.

24. (Currently Amended) A transponder as claimed in any claim 14~~any one of claims 14 to 20~~, wherein the transponder dynamically alters the maximum waiting time in response to an instruction from an interrogator.

25. (Currently Amended) A transponder as claimed in claim 14~~any one of claims 14 to 21~~, wherein the transponder is adapted to detect either heavy signal congestion or large quiet signal periods and alter the maximum waiting time accordingly.

26. (Currently Amended) A transponder as claimed in claim 14~~any one of claims 14 or 22~~, wherein the transponder is adapted to alter the maximum waiting time in response to an instruction from the interrogator or in response to external conditions present during the interrogation.

27. (Currently Amended) A transponder ~~including~~ comprising:

a receiver for receiving an interrogation signal from an interrogator;~~,~~

a transmitter for transmitting a response signal after receipt of the interrogation signal;~~,~~

means for generating the response signal during a waiting period; and

a random number generator the binary output signals from which are fed to the inputs of a counter for determining the waiting period, ~~characterised in that~~, wherein at least one of the output signals from the random number generator is fed via logic circuitry to a respective input of the counter, wherein ~~whereby~~ control of the logic circuitry adjusts the maximum length of the waiting period during interrogation by the interrogator.

28. (Cancelled).

29. (Currently Amended) A transponder as claimed in claim 14 ~~or any one of claims 16 to 25 when dependent on claim 14~~, wherein the random number is derived by taking a snapshot of the transponder clock, or by a hash value received from a command from an interrogator.

30. (Currently Amended) A transponder as claimed in ~~any one of claims 14 to 26~~claim 14, wherein the counter is an up or a down counter whereby the terminal value of the counter is reached with the clocking signal causing the counter to either increment or decrement as required.

31. (Currently Amended) A transponder as claimed in claim 14~~any one of claims 14 to 27~~, including a memory for storing an identity or data field and a modulator for transmitting the identity or data as a message in the output response signal.

32. (Currently Amended) An identification system comprising an interrogator and a plurality of transponders, the interrogator including a transmitter for transmitting an interrogation signal to the transponders, each transponder including a receiver for receiving the interrogation signal, a transmitter for transmitting a response signal after receipt of the interrogation signal and means for generating the response signal during a waiting period, each transponder having means for altering the maximum length of the waiting period during interrogation of the transponders by the interrogator, the transponder including a random number generator the binary output signals from which are fed to the inputs of a counter for determining the waiting period, ~~characterised in that~~ wherein at least one of the output signals from the random number generator is fed via logic circuitry to a respective input of the counter whereby control of the logic circuitry adjusts the maximum length of the waiting period.

33. (Currently Amended) An identification system comprising an interrogator and a plurality of transponders, the interrogator including a transmitter for transmitting an interrogation signal to the transponders, each transponder including a receiver for receiving the interrogation signal, a transmitter for transmitting a response signal after receipt of the interrogation signal and

means for generating the response signal during a waiting period, each transponder having means for altering the maximum length of the waiting period during interrogation of the transponders by the interrogator, the transponders having means for deriving a random number within the transponder and delivering the random number by way of binary output signals along a plurality of data lines to a counter, ~~characterised in that~~ wherein at least one of the data lines is connected to the counter via logic circuitry whereby control of the logic circuitry can block or permit the data line signal to the counter thereby adjusting the total number of data line signals reaching the input of the counter to control the maximum length of the waiting period.

34. (Cancelled).

35. (Currently Amended) An integrated circuit for use in a transponder of an RFID interrogation system, the integrated circuit comprising:

a receiver for receiving an interrogation signal;~~,~~

a transmitter for transmitting a response signal after receipt of the interrogation signal;~~,~~

means for generating the response signal during a waiting period and control means for altering the maximum length of the waiting period;~~, characterised by~~

means for deriving a random number within the integrated circuit and delivering the random number by way of binary output signals along a plurality of data lines to a counter and wherein at least one of the data lines is connected to the counter via logic circuitry control of which can block or permit the data line signal to the counter thereby adjusting the total number of data line signals reaching the input of the counter to control the maximum length of the waiting period.

36. (Currently Amended) An integrated circuit for use in a transponder comprising: ~~including~~

a receiver for receiving an interrogation signal;~~,~~

a transmitter for transmitting a response signal after receipt of the interrogation signal; ~~and~~

means for generating the response signal during a waiting period; ~~and~~

control means for altering the maximum length of the waiting period during interrogation of the transponder by the interrogator, a random number generator the binary output signals from which are fed to the inputs of a counter for determining the waiting period;~~, characterised by~~

a logic circuitry, wherein ~~whereby~~ at least one of the output signals from the random number generator is fed via the logic circuitry to a respective input of the counter, control of the logic circuitry thereby providing means for adjusting the maximum length of the waiting period.

37. (Currently Amended) An integrated circuit as claimed in claim 32~~ or claim 33~~, wherein the logic circuitry comprises one or more logic gates, the number of logic gates being less than the number of data lines for the binary output signals to the counter.

38. (Currently Amended) An integrated circuit as claimed in ~~any one of claims 32 to 34~~claim 32, wherein the waiting period consists of a plurality of smaller time intervals or time slots together defining a Round Size representative of that waiting period.

39. (Original) An integrated circuit as claimed in claim 35, wherein there is a minimum Round Size and at least one larger Round Size, the or each larger Round Size consisting of a combination of minimum Round Sizes, whereby controlling the logic circuitry determines the number of minimum Round Sizes to be combined to define the desired larger Round Size to be used.

40. (Currently Amended) An integrated circuit as claimed in claim 32~~any one of claims 32 to 36~~, wherein the logic circuitry is arranged to enable the maximum duration of the waiting period to be increased or decreased by multiples of 2 or 0.5 respectively.

41. (Original) An integrated circuit as claimed in claim 36, wherein the logic circuitry is arranged to enable the desired Round Size to be selected by increasing or decreasing the number of minimum Round Sizes to be combined, the different Round Sizes available being related to one another by factors or multiples of 2 or 0.5.

42. (Currently Amended) An integrated circuit as claimed in claim ~~32 or any of claims 34 to38 when dependent on claim 32~~, wherein the random number is derived by taking a snapshot of the transponder clock, or by a hash value received from a command from an interrogator.

43. (Currently Amended) An integrated circuit as claimed in claim 32 ~~any one of claims 32 to 39~~, wherein the counter is an up or a down counter whereby the terminal value of the counter is reached with the clocking signal causing the counter to either increment or decrement as required.

44. (Currently Amended) An integrated circuit as claimed in claim 32 ~~any one of claims 32 to 40~~, including a memory for storing an identity or data field and a modulator for transmitting the data in the output response signal.

45. (Currently Amended) A reader for identifying a plurality of transponders, the reader comprising:

a transmitter for transmitting a reader signal to the transponders;~~,~~

a receiver for receiving response signals from each transponder at a time within a respective waiting period the maximum duration of which can be adjusted;~~,~~ and

a processor for identifying a transponder from data in the response signal, ~~characterised in that~~

wherein the reader comprises detection means for detecting the number of collisions between response signals received at the receiver and control means for controlling the reader signal to control logic circuitry connected to a counter in the transponder to adjust the maximum length of the waiting period.